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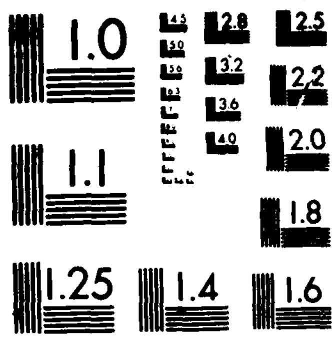
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AN EXPERIMENT ON INTERMITTENT-FAILURE MECHANISMS

Mario L. Côrtes and Edward J. McCluskey

CRC Technical Report No. 87-7
(CSL TR No. 87-322)

March 1987

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ABSTRACT

Intermittent failures are studied by stressing (temperature, supply voltage and extra loading) good parts. The behavior of the chips under stress is similar to that of a marginal chip under normal operating conditions. The experiments show that most intermittent failures are pattern-sensitive for both sequential and combinational circuits. The stuck-at fault model is shown to be inappropriate to describe intermittent failures. This paper presents a case where a single intermittent failure is not detected by a test set with 100% single stuck-at fault coverage. A stress-strength analysis is presented to explain the experimental results.

KEYWORDS: intermittent failures, pattern sensitive faults, soft failures, integrated circuit reliability, intermittent fault model.

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1 INTRODUCTION

Temporary failures are a major cause of digital system malfunctions. Two types of temporary failures can be identified [McCluskey 81, 86]: transient and intermittent failures. A **transient failure** is a nonrecurring temporary failure usually caused by external sources such as radiation, power supply fluctuation, etc. An **intermittent failure** is a recurring temporary failure that reappears on a regular basis caused by component degradation or poor design (violation of operating margins). The causes of intermittent failures are internal to the circuit. This paper discusses only intermittent failures.

Intermittent Failures (I.F.) are difficult to observe and control. This paper describes techniques to induce I.F. in digital circuits. Intermittent Failures are induced by stressing (temperature, supply voltage and loading) fault-free ICs (LSTTL and HCMOS). Supply voltage and temperature stresses affect gate noise immunity. Loading stress reduces the drive capability and simulates leakage paths. The stresses change the voltage transfer characteristics of gates in the circuit. The use of leakage paths to inject failures into CMOS integrated circuits has been reported in the literature [Levy 77]. All stresses used in the experiments have some impact on the communication between two gates, thereby causing the circuit under stress to exhibit a similar behavior to that of a marginal circuit under normal operating conditions. Preliminary results of this research were published in [Côrtes 86c].

Experimental results reveal an interesting behavior of I.F. in both combinational and sequential circuits: **Pattern Sensitivity**. Unlike the classical stuck-at faults, the occurrence of pattern-sensitive faults depends not only on the logic value at the fault site but also on the logic values of other lines in the circuit. The results show that the stuck-at fault model is not appropriate to describe intermittent failures. A case is presented where a single intermittent failure is not detected by a test set with 100% single stuck-at fault coverage. In situations like this, testing techniques that are based on more general fault models produce much better results. Exhaustive and pseudo-exhaustive testing are examples of such techniques.

The following paragraphs summarize the literature on intermittent failures and pattern sensitivity. Sections 2 and 3 present the experimental results. Section 4 presents a simple stress-strength analysis for the I.F. Additional data is presented in the Appendices.

I.F. modeling and testing. Several papers have addressed the problem of testing for intermittent failures. [Breuer 73], [Kamal 74], [Koren 77], [Varshney 79], [Stiffler 80] and [Savir 80] are some examples. The I.F. are described by Markov models. These papers use the following assumptions for the I.F.:

- Signal Independence: the periods of activity of the fault are independent of what signals appear in the circuit.
- Faults are well behaved: a fault is well behaved if, for a given clock cycle, either the circuit is fault-free or it behaves as if the fault is permanent for that clock cycle.

The assumptions of signal independency and randomness appear inappropriate in view of the experimental evidence of pattern sensitivity in intermittent failures.

Experimental Data. An attempt to collect data on intermittent failures on Sperry-Univac computers is reported in [O'Neil 80]. Hard failures (field data) that are believed to have appeared earlier as intermittent failures are analyzed. Two classes of failure mechanisms are listed as responsible for this type of failure: 1) metal-related open and short circuits; 2) marginal operation or violations of operating margins. The latter class of failures is the one studied in this paper.

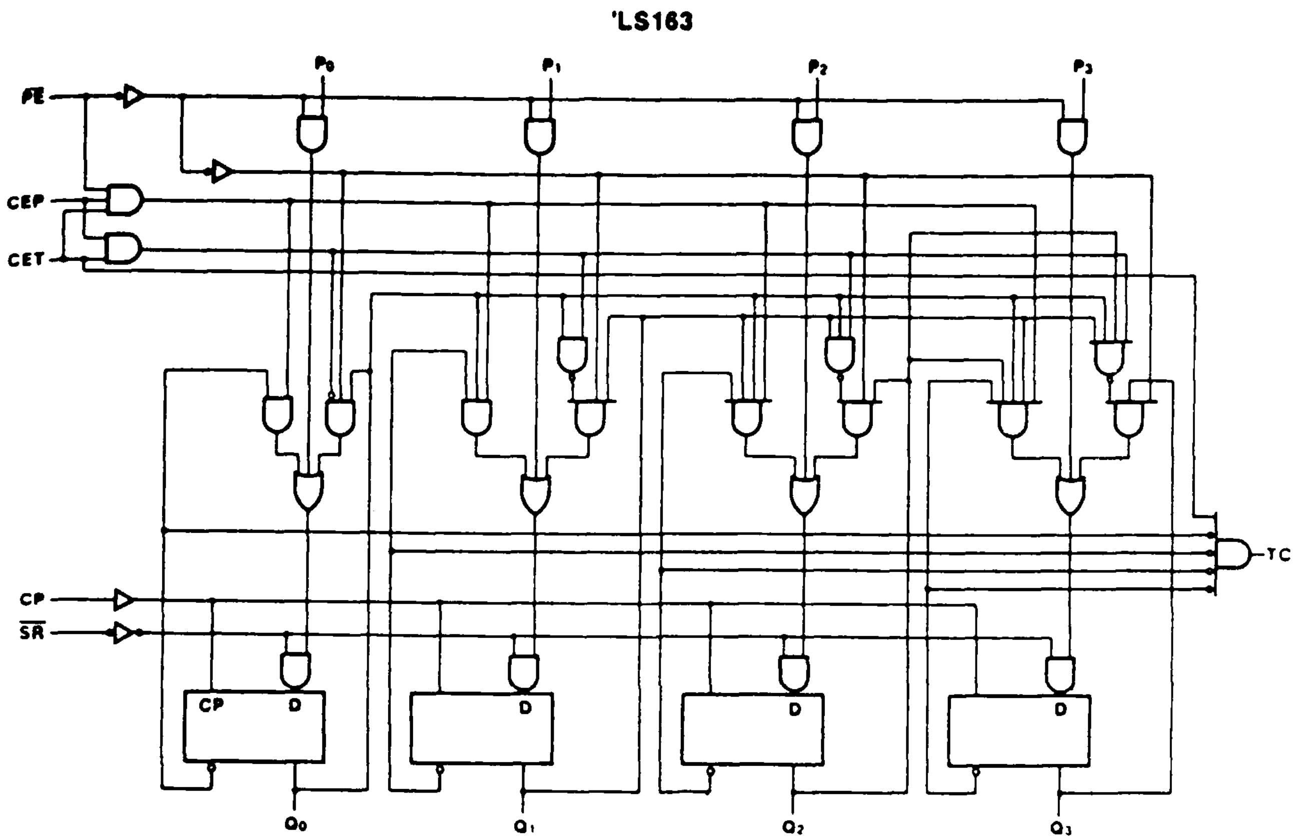
Pattern Sensitivity . Pattern Sensitivity was first reported in memory testing ([Reese-Brown 72], [Hayes 75, 80a]). [Rinerson 77] presents an interesting discussion on the causes of pattern sensitivity. [Hackmeister 75] reports instruction sensitivity in microprocessor chips. Using standard microprocessor characterization techniques, as described in [Healy 81], Hackmeister produced Shmoo plots (supply voltage versus speed) that have different shapes for different instruction streams. Other authors referred to Hackmeister results as pattern sensitivity due to "charge-leakage possibilities" [Bennetts 81] or "presence of moderately large RAMs on chip" [Hayes 80b]. Despite the lack of a detailed description of the experimental procedure in [Hackmeister 75], there is reason to believe that the failures are better described by delay faults than by pattern sensitivity. It is reasonable to conjecture that different instruction streams exercise different portions of the chip and failures are caused by delay faults due to supply voltage reduction as described in [Côrtes 86a, b]. In another paper, [Henley 84] refers to "pattern sensitivity" found in a RCA CMOS microprocessor (COSMAC 1802) that occurs only at operating frequencies higher than 4.0 MHz. The dependency on frequency suggests that this may be caused by a delay fault as well.

2 SEQUENTIAL CIRCUIT: BINARY COUNTER (74LS163)

The subjects of the experiment are 4-bit synchronous counters supplied by 4 different vendors. Bipolar (74LS163) counters are analyzed. Figure 1 shows a 74LS163 supplied by vendor A. The analyzed versions are pin compatible. The recommended operating conditions for the chips are power supply voltage in the range (4.75V - 5.25V) and temperature in the range (0°C - 70°C). This counter was a natural choice since another experiment [Côrtes 84] using 74LS163 counters (supplied by four vendors) at high temperature was already in progress.

The experiment consists of operating the counters in counting mode (SR' = PE' = CEP = CET =1) and applying voltage and temperature stresses to them. The faulty behavior is observed with a logic analyzer. Analysis at the logic and circuit levels are presented in this section. It is shown that the resulting intermittent failures are pattern sensitive. Circuit level analysis shows that failures are caused by excessive loading and diode leakage.

CMOS counters (74HC163) were also studied. No failures were observed at high temperature (120 °C) for supply voltages up to 6.6 V. In another experiment, run at room temperature and low supply voltage, only delay faults were observed. The use of low supply voltage is not appropriate to inject noise-immunity-type failures on CMOS chips because delay faults are dominant for all practical experimental conditions [Côrtes 86a, b]. Other failure-injection techniques are being considered.



Least Significant Bit

Most Significant Bit

Fig. 1: Binary Counter (74LS163; Vendor A)

2.1 Vendor A: High Voltage and High Temperature.

Many counters supplied by vendor A (Fig. 1) exhibit intermittent failures when operating at 118°C and supply voltage in the range (5.49V - 6.50V). The experiments are run on these counters under the conditions listed above and at 5.0 MHz. The counter outputs (Q_3 Q_2 Q_1 Q_0) are monitored with a logic analyzer. A number of error sequences can be observed for different levels of stress. Table 1 shows output sequences that can be observed under different levels of stress. Sequence I represents correct operation. When the stress level (voltage) is marginal, the behavior of the counter alternates between two sequences (Sequence IIa). For example, at 5.48V, the counter exhibits periods of correct operation (Sequence I) combined with periods of faulty operation (Sequence IIb). The occurrence of this intermittent failure is illustrated in Fig. 2.

Table 1: Output Sequences vs Vcc Range (Vendor A, 119 °C)

	Sequence	Vcc Range (V)
I:	....0123456789ABCDEF01....	3.50 - 5.48
IIa:	....9ABCD **ED...DE** F0....	5.48
IIb:	.... **EDEDED**	5.48 - 5.57
III:	....89ABCD **E5** 6789....	5.57 - 5.70
IV:	....89ABCD **E1** 23456789....	5.70 - 6.50

2.1.1 Logic-Level Analysis

Careful analysis of the circuit diagram shows that the classical stuck-at fault model is inappropriate for intermittent failures. It is shown that stuck-at faults occurring at random cannot describe the observed behavior. In all sequences, the incorrect state transition occurs when the initial state is E_{HEX} = 1110; in sequence II from E to D; in sequence III from E to 5; in sequence

IV from E to 1.

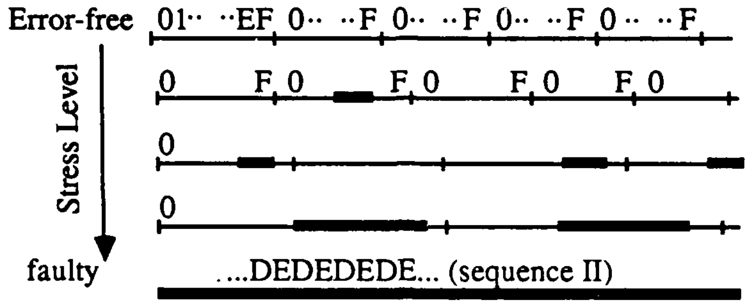
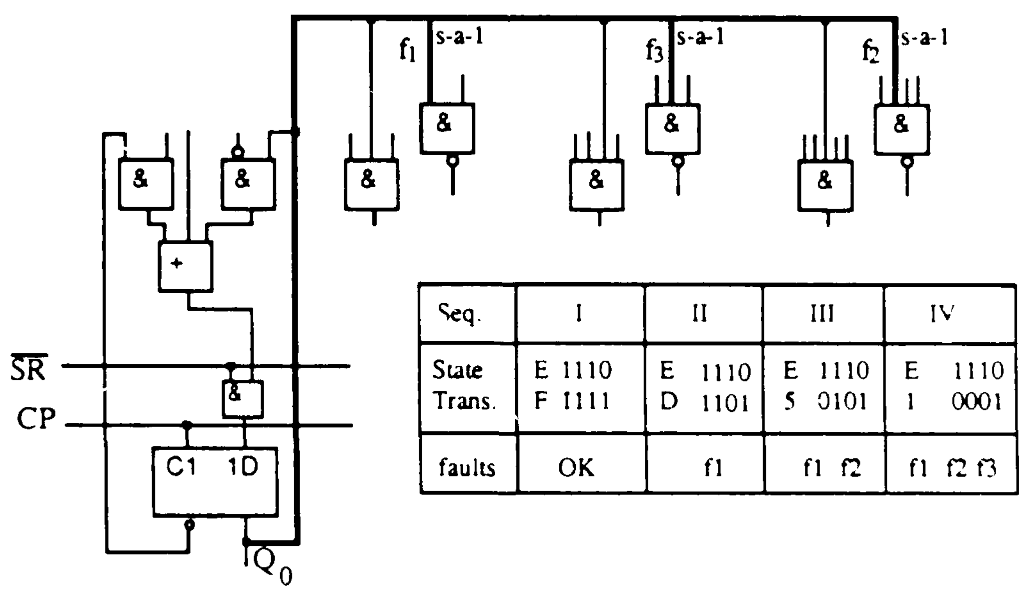


Fig. 2: Error Sequence type II for
Vcc between 3.50 and 5.57 V.

The incorrect transition can be explained by the inability of output Q_0 to correctly drive the 3 NAND gates in the circuit (Fig. 1). Let f1, f2 and f3 be faults defined as stuck-at-1 faults at the inputs of the NAND gates in the circuit. Figure 3 shows the circuitry driven by Q_0 and the location of the faults (f1, f2, f3).



Seq.	I	II	III	IV
State Trans.	E 1110 F 1111	E 1110 D 1101	E 1110 5 0101	E 1110 1 0001
faults	OK	f1	f1 f2	f1 f2 f3

Fig.3: Location and Fault Description of
the Intermittent Failure.

The incorrect transitions from state E can be explained by the following combinations of these faults: Incorrect transition E to D is due to fault f1. Incorrect transition E to 5 is due to the multiple fault f1 and f2. Incorrect transition E to 1 is due to the multiple fault f1, f2 and f3. These stuck-at faults explain the incorrect state transitions but not the complete faulty sequences. Should faults occur at random, one would eventually get other incorrect state transitions as well. For example, if fault f1 occurred at random, in addition to incorrect state transitions from E to D one would also expect to observe other transitions such as from A to 9 and from 4 to 7. The observed sequences can be explained only if there is some kind of **pattern sensitivity**, that is, the faults are active only when the counter state is equal to E_{HEX}. This explanation is supported by two facts: 1) One of the effects of high temperature on voltage transfer characteristics is the reduction of the low-input voltage (V_{IL}) [McCluskey 86], [Fairchild 78], [Prince 80]. 2) DC measurements of the Q_0 output voltage (which is driving the node 1 in Fig. 1) shows that the low-output voltage (V_{OL}) is maximum when the counter state is E_{HEX} (Table 2). The reason for the variation in V_{OL} will become clear in the circuit-level analysis (Sec. 2.1.2).

Table 2: V_{OL} at Q_0 for different counter states

V_{OL} (mV)	113	135	128	149	124	142	137	158
State (Hex)	0	2	4	6	8	A	C	E

The fault is located exactly at a point in the circuit where the load (fan-out) is maximum. Q_0 is loaded by 7 internal gates in addition to the external load (Fig. 1). Counters supplied by vendors B, C and D do not have gates as heavily loaded as the one in Fig. 1 and operate properly at the same stress level. This suggests that loading can influence fault activity. Analysis at the circuit level explains why state E is the most susceptible to failure and why the faults occur in the observed sequence.

2.1.2 Circuit-level Analysis

This section shows that the faulty behavior is due to excessive loading and increased diode leakage-current under temperature stress. The goal of this analysis is to show why faults (f1, f2, f3) may occur at state E and to explain the fault location and order of appearance. The logic-level analysis shows that the faulty behavior is related to the circuitry driven by Q_0. Figure 4 shows the electric diagram of the circuits driven by Q_0 in the counter (74LS163) supplied by vendor A. EN1 and EN2 are enable signals that determine the operation mode of the counter: in counting mode EN1 = EN2 = 1. The circuit shown in Fig. 4 decodes the current state (Q_3, Q_2, Q_1, Q_0) and generates the next state variables (Y_3, Y_2, Y_1, Y_0), that are applied to the flip-flops. The functions implemented by the transistors are:

$$Y_3 = Q_3 \oplus (Q_2\, Q_1\, Q_0)\,;\;\; Y_2 = Q_2 \oplus (Q_1\, Q_0)\,;\;\; Y_1 = Q_1 \oplus Q_0\,;\;\; Y_0 = Q_0'$$

The output of the least significant bit flip-flop (Q_0) drives the inputs of the combinational circuit (Fig. 4). The maximum load occurs when Q_0 alone is sinking current from the pull-up resistors at the transistor bases. The condition of maximum load occurs at state E (1110) because no other flip-flop (stages 1,2,3) is sinking current. This explains why the intermittent failure occurs at state E. This load analysis is straightforward if the circuit diagram is used. However, one can reach a different conclusion as to which state presents the highest load to Q_0 if the logic diagram is used for the analysis, because there is no direct correspondence between the logic diagram (Fig. 1) and the circuit diagram (Fig. 4).

The following paragraphs explain why faults f1, f2 and f3 appear successively. Figure 5 shows a simplified version of Fig. 4 where the inputs are set to EN1 = EN2 = $Q_3 = Q_2 = Q_1 =$ 1. These are the conditions when the counter is in counting mode and the state is E. In Fig. 5, some Schottky diodes are replaced by arrows representing the diode reverse currents. Transistors

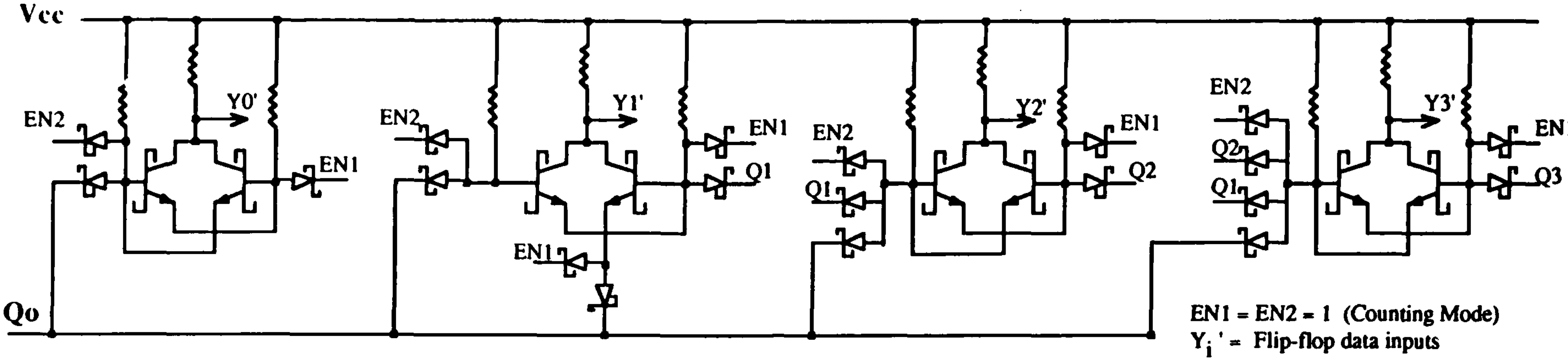


Fig. 4: Combinational part of 74LS163
(Vendor A, counting mode); circuits driven by Qo.

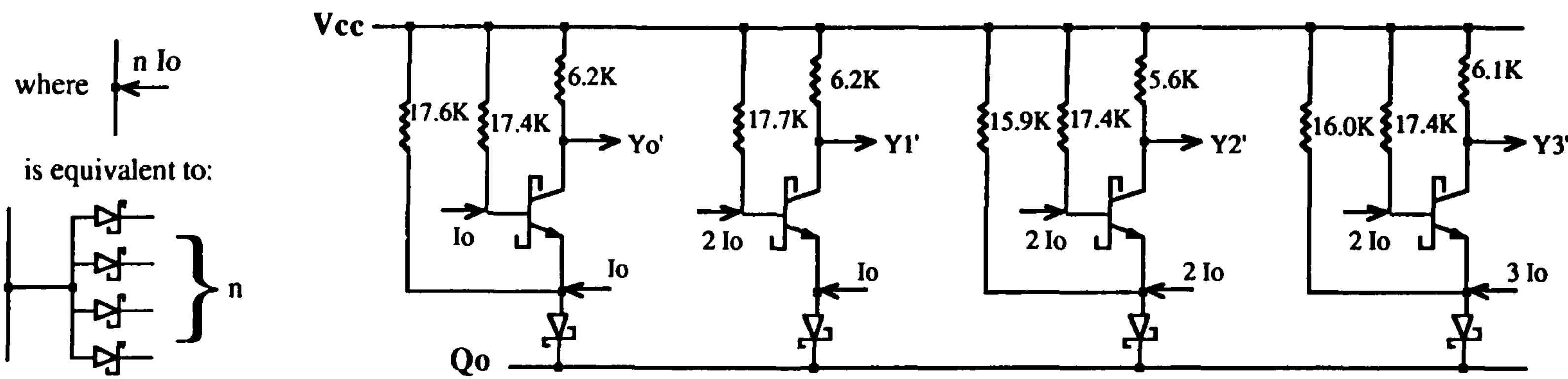


Fig. 5: Simplified circuit diagram for
counting mode and output state = E;
(Q3,Q2,Q1,Q0) = (1110)

operating in the cutoff region are not shown.

As the voltage level at Q_0 increases, the second least significant bit is the first stage to fail because it has the largest base resistor (17.7 K). Thus, the transistor in this stage receives the smallest base current and that is the reason why fault f1 (Fig. 3) occurs first.

The order of appearance of f2 and f3 is related to resistor values and diode leakage currents. In the analysis of the first batch from vendor A, faults occurred in the order f1, f2, f3, causing incorrect trasitions ED, E5 and E1 (Fig. 3). A second batch of chips under similar stress conditions (supply voltage and temperature) showed incorrect transitions ED, E9 and E1, that can be explained by faults f1, f3, f2. Parameter variations in the fabrication process are responsible for the different electric behaviors observed in batches 1 and 2. In one batch, f2 preceeds f3 and in the other, f3 preceeds f2.

Diode leakage current plays an important role in the counter behavior at high temperature. There is a 3 orders of magnitude increase in the reverse current as the temperature rises from 25 °C to 125 °C. Reverse currents (Io) for Schottky diodes at 125 °C are in the range (0.1 to 10 mA) [Hodges 82] [Sharma 84].

Experiments on the 74LS163 show that without the temperature stress (increased leakage current) there is still a dependency of $V_{OL}(Q_0)$ on the counter state (as shown in Table 2). However, the change in $V_{OL}(Q_0)$ alone is not sufficient to cause errors. Figure 5 shows diode reverse currents, represented by arrows (Io, Io, 2Io, 3Io). When Q_0 is low, it is responsible for sinking the currents coming from all stages, including the reverse currents. The increased magnitude of the reverse currents accounts for the increase of $V_{OL}(Q_0)$ at high temperature, which is the source of error. The order of occurrence of f2 and f3 is determined by circuit parameters (resistor values) and by the amount of reverse current per stage (2Io, 3Io).

2.2 Low Voltage, Room Temperature

Counters supplied by vendors B, C and D operate correctly for supply voltages up to 6.60 V and temperatures up to 126°C. In order to compare the behavior of counters from different vendors, another experiment was run using low supply voltage as stress. The experiment was run at room temperature and at 150 Hz. By running the experiment at such a low frequency, the effects of supply voltage on propagation delay were guaranteed not to cause errors [Côrtes 85, 86]. Therefore all observed errors can be attributed to noise immunity violations. Delay faults in the counters produce a different behavior (Appendix A.1). Table 3 shows the results for 150 Hz.

Table 3: IF caused by low supply voltage at room temperature, 150 Hz.

Vendor	Vcc (V)	Output Pattern
A	2.920	...0123456789ABCDF 01...
B	2.029	...89AB4 56789...
C	2.009	...01234567C DEF01...
D	2.246	...0123456789ABCF 01...

Analysis of the error sequences in Table 3 shows that counters from vendors A, C and D exhibit pattern-sensitive intermittent failures. Furthermore, it can be shown that in the latter case (vendor D), there exists a complete test set for the combinational part of the counter (see Sec. 2.2.2), based on the single stuck-at fault assumption, that does not detect the incorrect transition C to F. Section 2.2.1 presents an analysis of the results on Vendor A chips and Section 2.2.2 on Vendor D chips. Chips from Vendors B and C are analyzed in Appendix A.2.

2.2.1 Vendor A, Low Voltage, Room Temperature.

The pattern observed most frequently was DF (1101,1111). As the stress level increased (lower Vcc) other errors were observed as well. The incorrect state transitions, in order of appearance are: DF, 9B, 57, BD, 13, 35, 79, F1, BF, 37. At the lowest level of stress to cause error, the output sequence is ···89ABCDF0123····. For the next level of stress, the output sequence is ···456789BCDF0123····. When error F1 appears, the least significant bit is stuck-at-1 and the output sequence is ···**13579BDF**··· . The least significant bit stage is the first to fail and it consistently fails when the state is D. In up counters such as the 74LS163, the next state for the lower order bits does not depend on the current values of the higher order bits. The only reason for a failure to occur at a **specific state** in the **lowest order stage** is some kind of **pattern sensitivity**. The following paragraphs study the fault location (Q_0) and the susceptibility of the counter to voltage stress at various states.

Fault Location. As the supply voltage is reduced, one expects the first failure to occur on the path from Vcc to Gnd containing the largest sum of threshold voltage drops and resistances. In the counter from vendor A, this path consists of an inverter that takes as input the output of a pull-down network that evaluates the next state (Y_i') and generates the other data input (Y_i) to the flip-flop of that stage. The path in this circuit (Fig. 6) consists of 3 Schottky diodes, one junction diode (base-emitter diode) and the resistor R_i. The resistor values given in the electrical diagram are: R_3 = 6.1 KΩ; R_2 = 5.6 KΩ; R_1 = 6.2 KΩ; R_0 = 6.2 KΩ.

The failure mechanism is as follows: at a certain supply voltage level, the transistor base voltage is no longer sufficient to turn it on, causing (Yi Yi') = (1 1) which keeps the flip-flop at its previous state after one clock cycle. This occurs when current state is 1 and next state is 0. For the least significant bit this results in even states being skipped. In the two batches that were analyzed, stage Q_0 was the first to fail (R_0 = 6.2 K). One can expect stage Q_1 (R_1 = 6.2 K) to fail in other batches due to variations in resistor values and threshold voltages. In this experiment, stage Q_1 did fail (BF, 37) but that occurred only after Q_0 was already stuck-at-1.

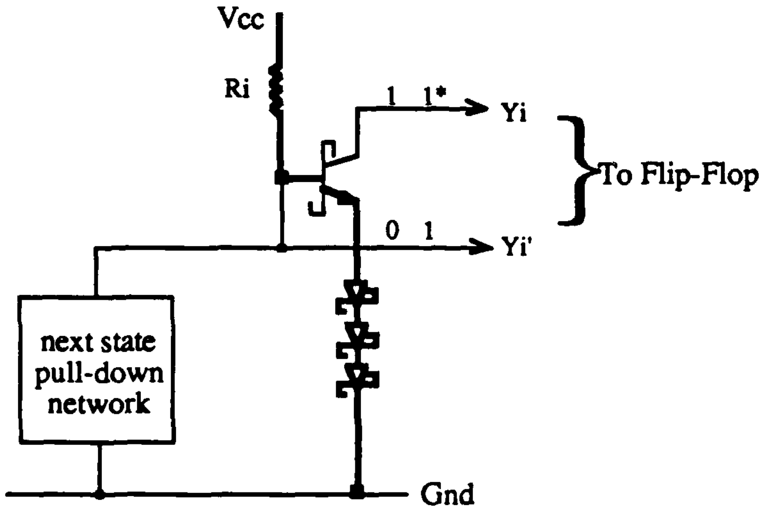


Fig. 6: Path to fail at low supply voltage, Vendor A.

State to Fail. It was found that, as the supply voltage is reduced, the first state to fail is the one drawing the largest supply current. Table 4 shows the current drawn by the counter for odd states ($Q_0 = 1$). The incorrect transitions for different levels of stress are also shown. The correlation is perfect.

Table 4: Correlation between supply current and state to fail.

State Icc current (mA)	D 1101 16.4	9 1001 15.7	5 0101 15.7	B 1011 15.4	1 0001 15.0	3 0011 14.6	7 0111 14.4
Supply Voltage (V) Incorrect Transition	2.86 DF	2.81 9B	2.80 57	2.79 BD	2.74 13	2.72 35	2.71 79

2.2.2 Vendor D, Low voltage, Room Temperature.

As shown in Table 3, the fault for the Vendor D chip consists of an incorrect transition from C to F. Fig. 7 shows a fault in stage B that can cause that behavior. The complete logic diagram is shown in Appendix A4. It will be shown that there exists a complete test set for the combinational part of the circuit, based on a single stuck-at fault assumption that does not detect the incorrect transition from C to F, because it does not contain the state C.

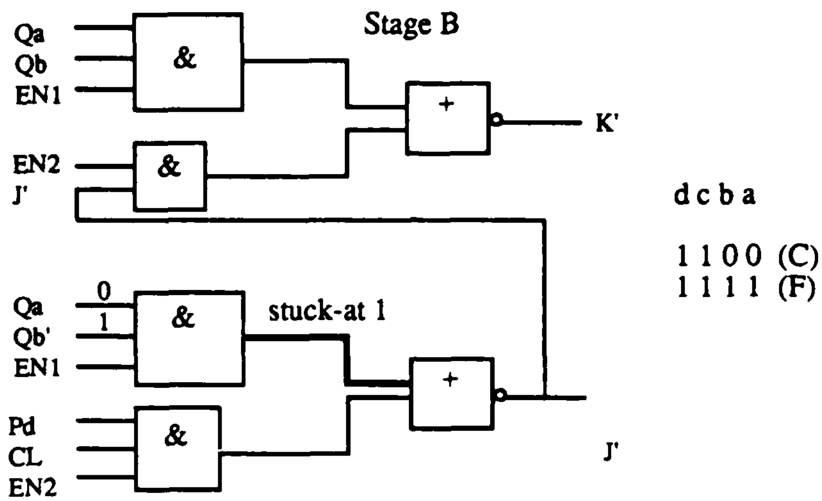
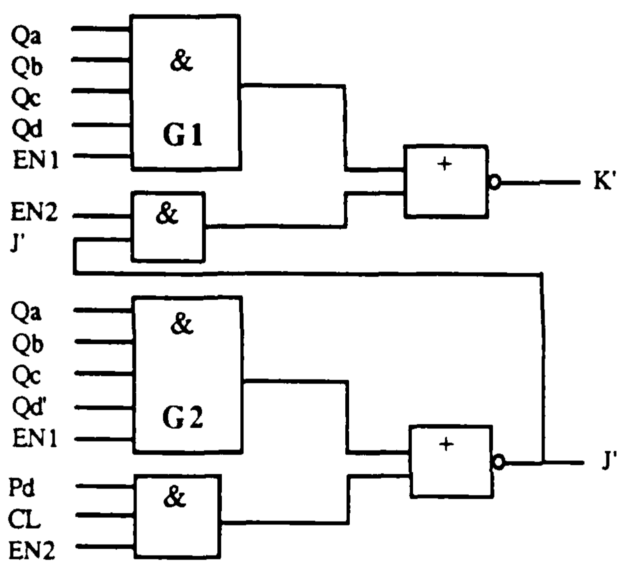


Fig. 7: Stuck-at 1 fault causing incorrect transition from C to F.

By examining the logic diagram of the counter, one can see that the combinational circuit of a given stage is a subset of the combinational circuit of higher order stages. Therefore, a test set for faults in the highest order stage (Q_D) is also a test set for the other stages (Q_C,Q_B,Q_A). Figure 8 shows the highest order stage circuitry and the set of all vectors that require specific combinations of state variables (Q_D,Q_C,Q_B,Q_A) to detect all single stuck-at faults at the 5-input AND gates. This set of combinations is essential and must be included in any complete test set. In addition to this test set, another set of vectors is necessary to test the counter load, enable and clear functions (NOR gates, 2-, 3-input AND gates). However, this additional set of vectors does not depend on the counter state and does not add any combinations of state variables to the already existing test set. Therefore, there exists a complete test set based on the single stuck-at fault assumption that does not contain state C.

This finding illustrates the situation when boards fail in the field and then pass diagnostics tests that are guaranteed to have a 100% single stuck-at fault coverage. This could be avoided by the use of exhaustive or pseudo-exhaustive testing techniques [McCluskey 86]. For this counter, pseudo-exhaustive testing detects the intermittent failure. Suppose gate G_1 (Fig. 8) is one of the segments after partitioning. Its inputs are EN_1, Q_d, Q_c, Q_b, Q_a. An exhaustive test for this gate contains all states, thereby detecting the incorrect transition from state C to state F. Pseudo-exhaustive testing is guaranteed to detect pattern-sensitive faults as long as the pattern sensitivity is not due to coupling between nodes located in different segments.



	Qd	Qc	Qb	Qa	
Test Set for **G1**	1	1	1	1	(F)
	0	1	1	1	(7)
	1	0	1	1	(B)
	1	1	0	1	(D)
	1	1	1	0	(E)
Test Set for **G2**	0	1	1	1	(7)
	1	1	1	1	(F)
	0	0	1	1	(3)
	0	1	0	1	(5)
	0	1	1	0	(6)

(Qd, Qc, Qb, Qa) in the complete test set:
3,5,6,7,B,D,E,F

Fig. 8: Complete combinational test set, not containing state C.

3 COMBINATIONAL CIRCUITS

This Section presents experimental results on the injection of intermittent failures in combinational circuits. The injected I.F.s are pattern sensitive in all experiments (LSTTL and HCMOS gates). It is shown that the I.F. occurrence depends ont only on the logic value at the fault site but also on the logic values at other lines in the circuit. In some cases, coupling via power supply noise was responsible for the pattern sensitivity of the I.F.s. In all experiments, clock frequency had no effect on the I.F. characteristics.

In this experiment, loading is used as a stress to disturb the communication between a driver and a receiver (Fig. 9). The stress can be adjusted to a level that causes marginally correct operation, leading to an intermittent-failure type of behavior. This type of I.F. is hereafter referred to as "light I.F.". The effect of additional load in a good circuit can also be related to the effect of leakage paths due to parameter degradation or fabrication defects in a marginal circuit, as reported in [Levy 77].

This Section presents experimental results and analysis for the logic gates: XOR gate 74LS86 (Sec. 3.1), NAND gate 74LS00 (Sec. 3.2), OR gate 74LS32 (Sec. 3.2) and XOR gate 74HC86 (Sec. 3.3).

3.1 XOR Gate 74LS86.

A first set of experiments uses a circuit based on XOR gates 74LS86 (Fig. 9). Input patterns X, Y, and Z are chosen to be 4-bit long vectors that exhaustively test all gates in the circuit. The loading disturbance is applied to node W (fault site). Different combinations of X, Y, and Z, producing the same logic signal at W, cause different error behavior at the output. The input patterns are applied at a rate of 2.0 MHz. Section 3.1.1 presents data for load to Vcc and

Section 3.1.2 presents data for load to Gnd.

3.1.1 Load to Vcc.

Table 5 shows XOR receiver output errors when an extra path to Vcc is present. The different input sequences at X, Y, Z are such that: 1) the XORs are exhaustively tested; 2) in all sequences, the logic signal at the fault site W is 0110. When load to Vcc is applied, one expects errors at the first and fourth bits applied. However, errors occur sometimes at the first and sometimes at the fourth bit (fault occurrence is shown in boldface in Table 5). Errors always occur when (XY) = (11). The reason is that V_{OL} at W is higher for (XY) = (11) than for (XY) = (00) (Table 6). The (00) input to the XOR provides a better pull-down capability.

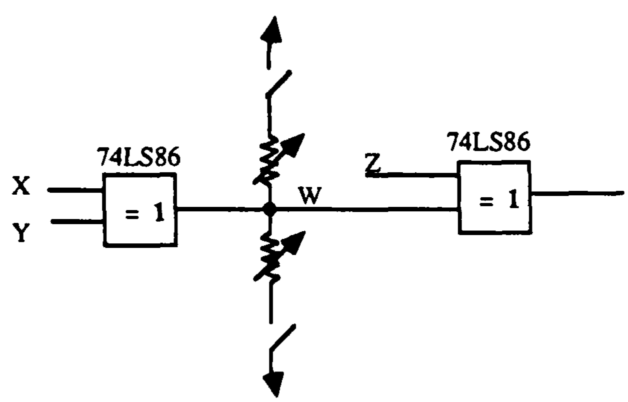


Fig. 9: Experimental Set-Up for Combinational Circuits

Table 5: Error Occurrence and Signal Dependency. Load to Vcc.

X Y Z W	Fault-free	Faulty with load to Vcc
0011 0101 0011 0110	0101	010**0**
1100 1010 0011 0110	0101	**1**101
0011 0101 1100 0110	1010	101**1**
1100 1010 1100 0110	1010	**0**010

Table 6: V_{OL} Versus Input Logic Signals.

Load to Vcc	XY W	V_{OL} at W (V)
No	1 1 0 0 0 0	0.195 0.161
Light	1 1 0 0 0 0	1.770 1.064
Strong	1 1 0 0 0 0	1.842 1.213

3.1.2 Load to Gnd.

A similar experiment was rur. with load to Gnd. Table 7 shows the results. One expects extra load to Gnd to cause errors at the second and third bits applied. Table shows that errors always occur when Z = 1. The reason for this dependency is that the voltage transfer characteristic (VTC) from W to the output is more susceptible to disturbances (at W) when Z = 1. Figure 10 shows the VTC for different levels of leakage (load) to Gnd. For light disturbances, the XOR exhibits correct operation for Z = 0 and faulty operation for Z = 1.

Table 7: Error Occurrence and Signal Dependency. Load to Gnd.

X	Y	Z	W	Fault-free	Faulty with load to Gnd
0011	0101	0011	0110	0101	0 1 **1** 1
1100	1010	0011	0110	0101	0 1 **1** 1
0011	0101	1100	0110	1010	1 **1** 1 0
1100	1010	1100	0110	1010	1 **1** 1 0

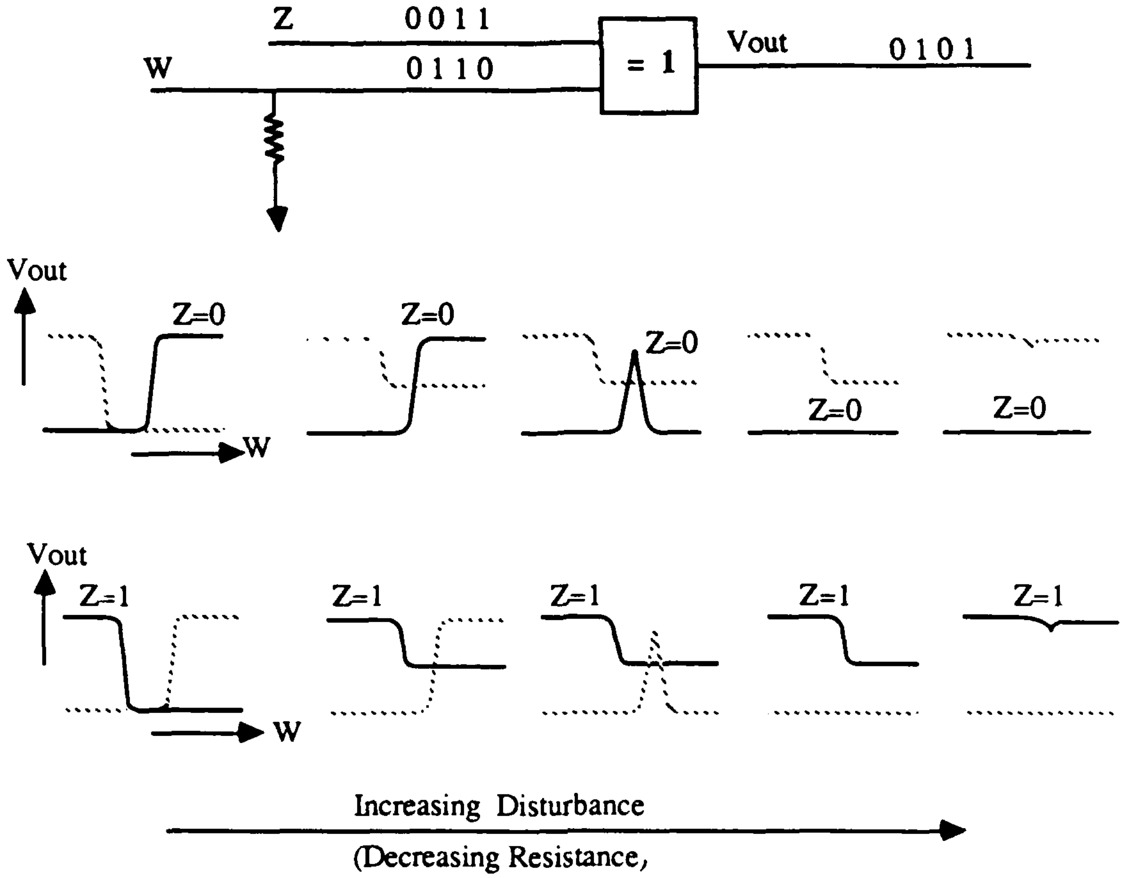


Fig. 10: Voltage Transfer Characteristic (VTC) from Input W to Output.

3.2 NAND Gate (74LS00) and OR Gate (74LS32)

In this experiment, the Z input is tied to 1 for the NAND gate and to 0 for the OR gate (Fig. 11). In this way, when an extra load is applied at W, faults can be observed at the output. Figure 11 shows the application of input vectors XY = (00), (01), (10), (11), denoted as 0123. These inputs produce W = 1110 for the NAND gate and W = 0111 for the OR gate.

The following experiment studies the effect of the order of application of all four possible combinations of XY on fault occurrence. The measurements are performed with logic analyzer samplings on rising and falling edges. It can be seen (Table 8) that analyzing the results is not as straightforward as in the case of the 75LS86 (Sec. 3.1). Table 8 shows the input vector (0,1,2,3) for which the circuit is the most sensitive to disturbances. The results depend strongly on how the vectors are applied (order of application) and how the measurement is performed (sampling at rising or falling edges).

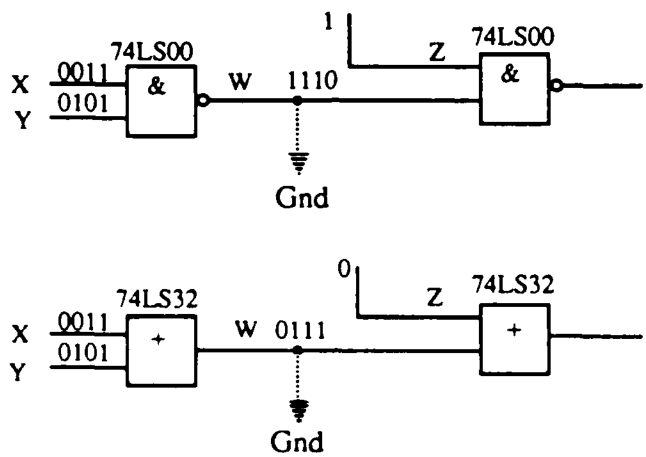


Fig. 11: Experimental set-up: load to Gnd on 74LS00 and 74LS32 gates.

Table 8: Error-occurrence State on 74LS00 and 74LS32 Gates
for Different Order of Application of Input Vectors.
Logic Analyzer Samples on Rising and Falling Edges.

Input Order	74LS00 Input Vector at Time of Failure ↑	74LS00 ↓	74LS32 ↑	74LS32 ↓
0123*	2	2	3	2
0213	1	0	1	1
0132	2	2	2	3
0312	1	1	1	1
0231	2	2	3	3
0321	2	2	2	3

f = 1.0 MHz

* 0123 stands for: (XY) = (00),(01),(10),(11)

A second experiment allows for better resolution in the observations. The data is sampled by the logic analyzer at a rate of 10 samples per clock period (Table 9). The faults occur at application of vectors 2 or 3 (10,11), whichever appears first. (Appendix A.3 shows all the waveforms observed on the oscilloscope). Figure 12 shows scope waveforms for a few sequences of inputs. Glitches in V_{out} indicates error occurrences. From Fig. 12, one can draw the following conclusions: a) failures occur at the rising edge of the clock; b) failures occur when input vectors 2 (10) or 3 (11) are applied; there is a glitch only for the first of these two vectors to be applied.

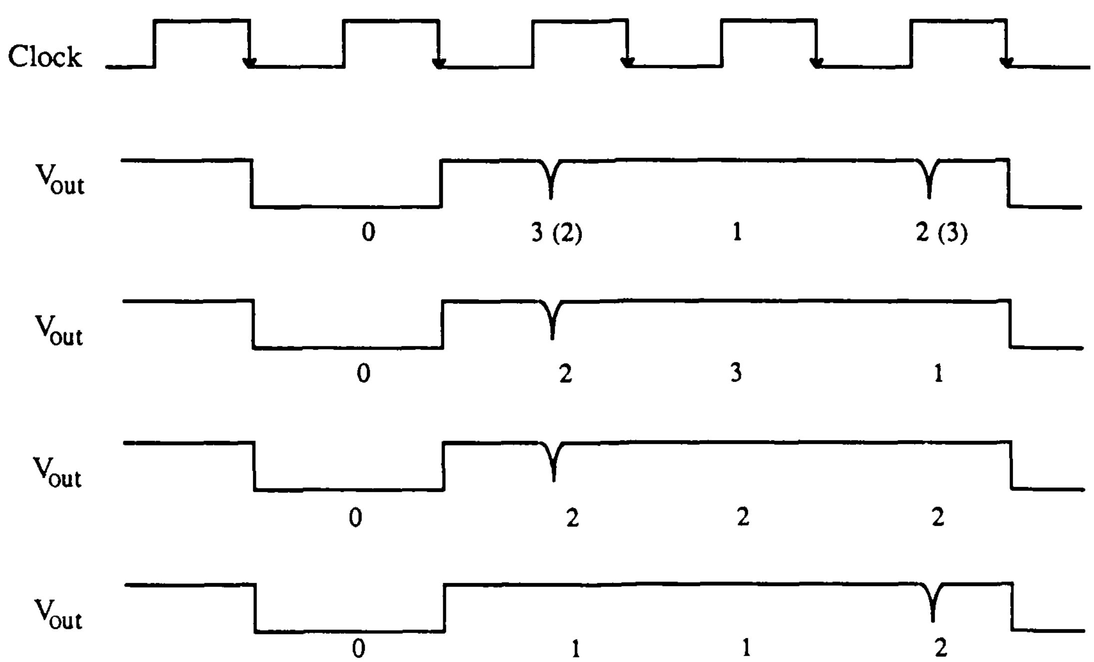


Fig. 12: Oscilloscope Waveforms at the Output of an OR Gate (74LS32) for Different Order of Application of Input Vectors. Glitches Show Error Occurrence.

Table 9: Error-occurrence State on 74LS32 Gates for Different Order of Application of Input Vectors. Logic Analyzer: 10 Samples per Clock Cycle.

Input Order	Input Vector at Time of Failure
0 1 2 3 *	2
0 2 1 3	2
0 1 3 2	3
0 3 1 2	3,2
0 2 3 1	2
0 3 2 1	3

Conditions:
- Load to GND
- f = 100 KHz
- sampling rate: 1.0 MHz

* 0123 stands for: (XY) = (00),(01),(10),(11)

Vectors are generated at the clock rising edge and applied to the circuit at the falling edge. Faults occur at the rising edge of the clock because power supply noise causes a dip on the supply voltage. Figure 13 shows the power supply noise, input vectors and clock waveform. The noise depends only on the generation of input vectors and does not vary as stress level is changed.

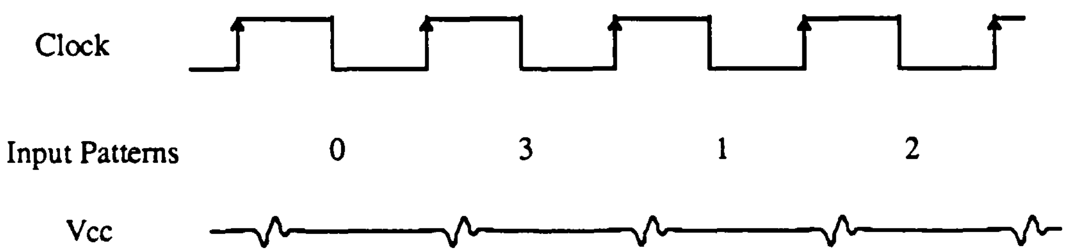


Fig. 13: Power Supply Noise and Clock Waveform.

The fault behavior can be summarized as follows. The faults are pattern sensitive. The fault occurrence is related to specific input vectors applied to the circuit. It is also coupled to signal transitions on other chips via power supply noise.

3.3 CMOS XOR Gate 74HC86

Table 10 shows the experimental results for load to Gnd and Vcc. The faulty bits are highlighted in boldface. For load to Vcc, the fault is provoked (logically) when W = 0, that is, in the first and fourth bits (W = 0110). However, faults occur only in the fourth bit. Similarly, for load to Gnd, faults occur only in the second bit (not in the third bit). Faults occur when W switches from 1 to 0 (load to Vcc) and 0 to 1 (load to Gnd). This is also caused by power supply noise, as shown in Fig. 14. In this case, the supply noise is strongly dependent on the stress level, and is due to local switching at the fault site, as opposed to the 74LS32 described in Sec. 3.2. The fault behavior can be summarized as follows. An extra path to ground (or Vcc) has the highest probability of causing an error at logic switching time.

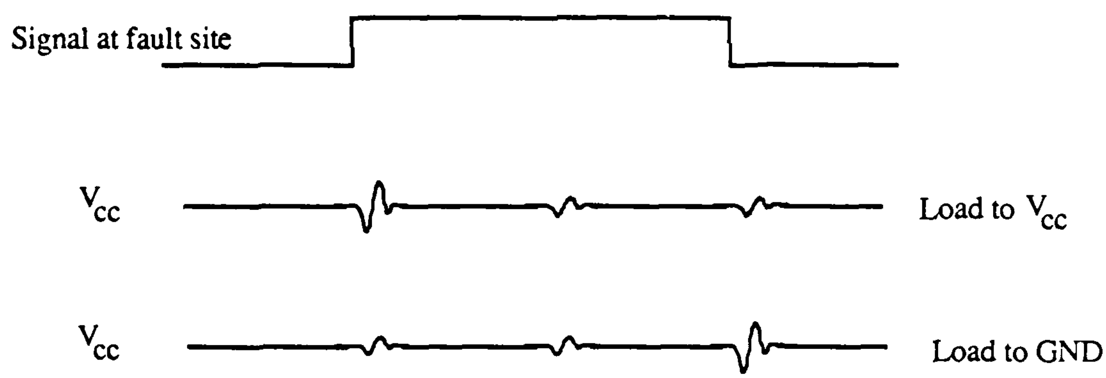


Fig. 14: Power Supply Noise Due to Leakage
(Extra Load) at the Fault Site; 74HC86.

Table 10: Faults on 74HC86 XOR Gates
for Load to Gnd and to Vcc.

X	Y	Z	W	Fault-free	Faulty ↑Vcc	Faulty ↓Gnd
0010	0101	0011	0110	0101	0100	0001
1100	1010	0011	0110	0101	0100	0001
0011	0101	1100	0110	1010	1011	1110
1100	1010	1100	0110	1010	1011	1110

3.4 Summary for Combinational Circuits

This Section summarizes the faults observed by applying extra load to combinational circuits and lists the sources of pattern sensitivity.

a) The driver ability to pull down a node is disturbed by a load to Vcc. Some input vectors provide a better pull-down capability to the driver (74LS86, Sec. 3.1.1).

b) The receiver voltage transfer characteristic is disturbed by load to Gnd at one of its inputs. The receiver is more sensitive to disturbances for some input vectors (74LS86, Sec. 3.1.2).

c) Faults are provoked (logically) by three input vectors but only two of them cause errors. The error occurrence is coupled to logic transitions at other locations on the board via power supply noise (74LS32, Sec. 3.2).

d) Faults occur only when there is a logic transition at the fault site. The fault is caused by a voltage dip at the power supply line (74HC86, Sec. 3.3).

4 STRESS-STRENGTH ANALYSIS

This section presents a stress-strength analysis similar to the ones used by mechanical reliability engineers [Dhillon 81]. The model describes the signal-dependent faults observed experimentally. Figure 15 shows a general driver-receiver pair. The I.F. due to marginal operation is caused by some error in the interface between the driver and the receiver (line W). It was shown that I.F. are pattern sensitive or signal dependent. This is illustrated in Fig. 15 by taking a set that contains all test vectors for a stuck-at fault at fault site W. The I.F. is pattern sensitive if there is at least one vector in the set that does not detect the fault. Pattern sensitivity is due to the fact that it is not sufficient to specify the **logic value** at the fault site in order to provoke the fault. For a pattern sensitive I.F., provoking the fault requires **voltage/current level** conditions at the fault site and this may be a function of the overall state of the circuit. In this paper it was shown that driver and receiver input conditions are "coupled" to the I.F. occurrence. One expects other signals like Yi (Fig. 15) and power supply noise to contribute as well. The stress strength analysis provides a qualitative framework to understand the I.F. pattern sensitivity.

In this analysis, V_{IL}, V_{IH} at the receiver input can be related to strength and, V_{OL}, V_{OH} at the driver output, to stress. A failure occurs when stress is larger than strength. Stress (driver output characteristics) can be increased by circuit degradation, supply voltage fluctuation, temperature, crosstalk, electromagnetic interference and driver input conditions (Xi in Fig. 15). Strength (receiver input characteristics) can be reduced by circuit degradation, temperature, supply voltage fluctuation and receiver input conditions (Zi in Fig. 15).

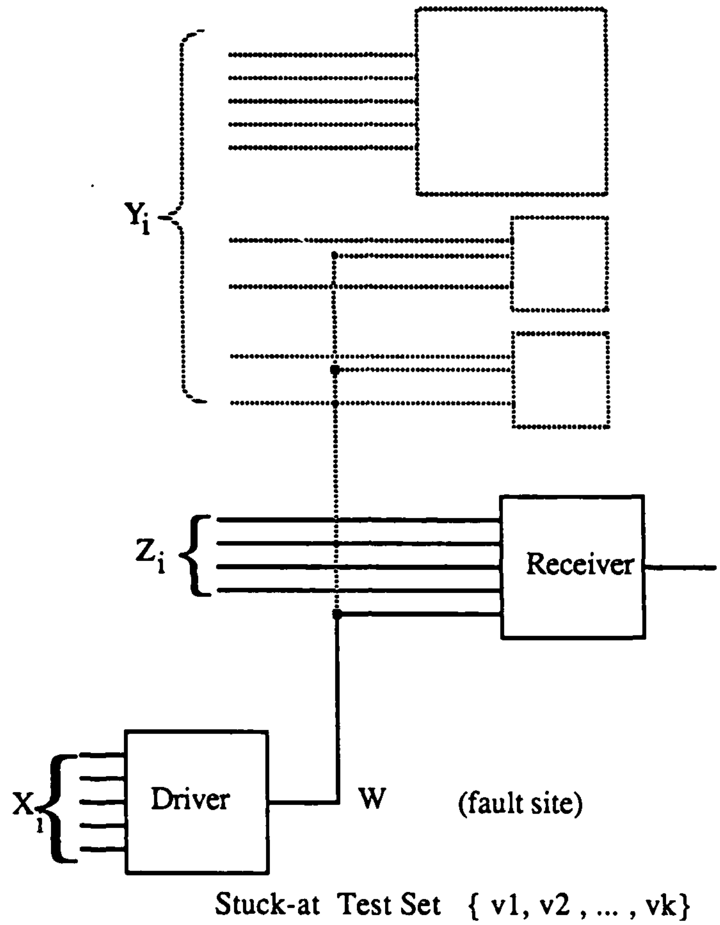
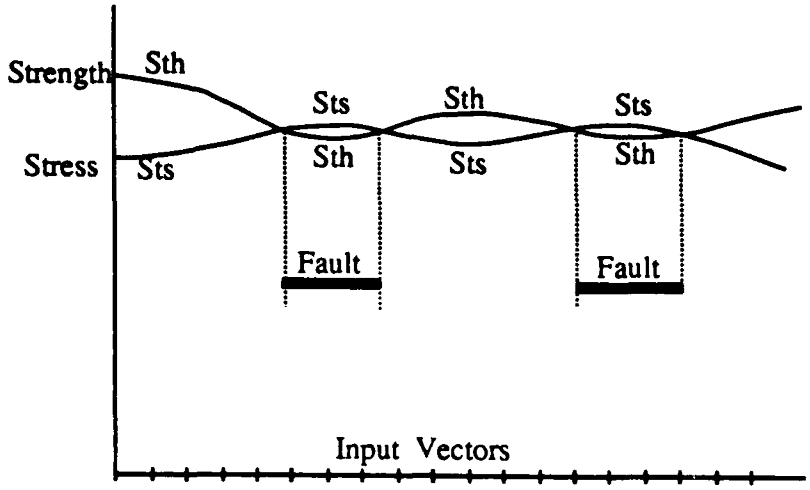
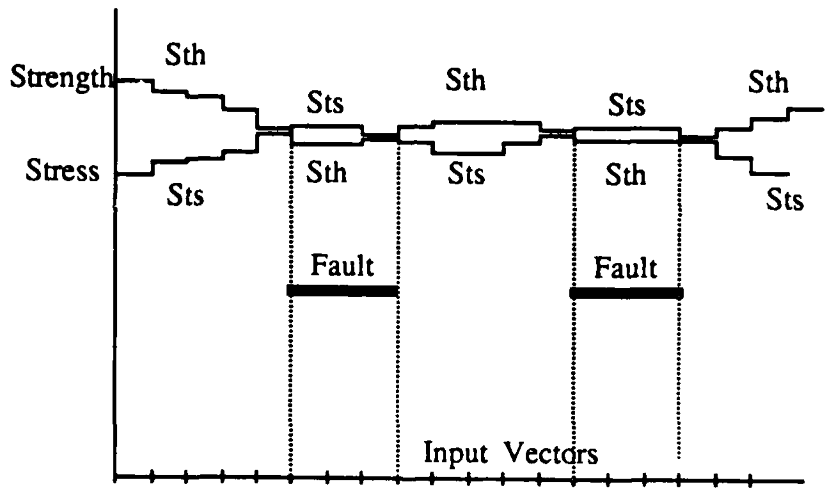


Fig. 15: Driver-Receiver Pair

The important feature of the model is the dependency on input conditions. Figure 16 shows the stress-strength model for signal independent (a) and signal dependent (b) situations. In the former, stress and strength are random variables and in the latter, they are "modulated" by the input conditions. The signal-dependent stress-strength model illustrates the interaction between the variables involved in the process. The model also provides an explanation for the fact that most IFs observed in the measurements change state from active to inactive, or vice versa, exactly at data transition times, as shown in Fig. 16b).



(a) Signal Independent



(b) Signal Dependent

Fig. 16: Stress-Strength Analysis.

It is believed that, to some extent, the input conditions always have some impact on stress and strength. Therefore, it is reasonable to conjecture that light IFs are pattern-sensitive in nature, not only for the LSTTL and HCMOS catalog parts studied here but for all other technologies.

5 SUMMARY AND CONCLUSIONS

Intermittent failures are studied by stressing (temperature, supply voltage and loading) good parts. The circuits under stress exhibit a similar behavior to that of a marginal circuit under normal operating conditions. The experiments reveal the existence of pattern-sensitive I.F., for both sequential and combinational circuits. The pattern sensitivity is particularly strong for IFs with low probability of activity (marginal overlap between stress and strength curves in Fig. 8). This finding contradicts the assumption of signal independence and randomness in the fault models used by I.F. testing techniques. The results show that stuck-at faults are not an appropriate model for IFs. A case is presented where a single intermittent failure is not detected by a test set with 100% single stuck-at fault coverage for faults in the combinational part of the circuit. In situations like this, testing techniques that do not rely on fault models produce much better results. Exhaustive and pseudo-exhaustive testing are examples of such techniques.

The techniques presented in this paper represent a valuable tool not only to study intermittent failures but also to inject realistic failures in digital circuits in order to evaluate fault-tolerant systems and checking circuits. Experiments along these lines are in progress and the results will be published soon.

Pattern sensitivity is a direct result of the marginal nature of IFs. Although the experiments were performed on LSTTL and HCMOS catalog parts only, it is reasonable to extend the results to other technologies. Additional experiments on counters and other combinational logic circuits are still in progress and will be reported in a separate paper.

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APPENDIX A.1

Delay Faults in 74LS163 Counters

This experiment was performed to make sure the behavior observed at low voltage, reported in Table 3, was not due to delay faults. Chips supplied by Vendors A and D were used. The experiments were run at 30 MHz. The maximum operating frequency is 25 MHz for Vendors A and D. Table A.1 shows the results. It can be seen that faults at 150 Hz are due to noise immunity problems.

Table A.1: Incorrect Transitions at Room Temperature for the 74LS163.

Vendor	f = 150 Hz		f = 30 MHz	
	Incorrect transition	Vcc (V)	Incorrect transition	Vcc (V)
A	DF	2.92	13	4.30
D	CF	2.25	66	4.26
	noise immunity		delay fault	

APPENDIX A.2

Vendors B and C; Low Voltage, Room Temperature.

Vendor C. Counters from Vendor C exhibit incorrect transitions from 7 (0111) to C (1100) (Table 3). The fault is located in bit Q_2 (stuck-at 1, for state 7); the correct next state is 8 (1000). Error = 8 $\oplus$ C = 1000 $\oplus$ 1100 = 0100. It is a pattern sensitive fault because the stage at which it occurs is not the highest order one. The explanation presented in Section 2.2.1 holds here, as well.

Vendor B. Counters from Vendor B exhibit incorrect transition from B (1011) to 4 (0100) (Table 3). The error is C $\oplus$ 4 = 1100 $\oplus$ 0100 = 1000, located at the highest order stage. Fig. A.2 shows part of the logic diagram in stage Q_3 and a table with a more complete description of the behavior. The fault X_3 / 1, responsible for the incorrect transition from B to 4 **is not** pattern sensitive because B (1011) is the only vector to correctly provoke and sensitize the fault. An interesting aspect of the behavior of this counter under low voltage is the fact that all faults appear at the input of the AND gate. This means that the voltage stress affects the receiving characteristics of that gate.

	1st failure @ 2.029 V	2nd failure @ 2.016 V	3rd failure @ 2.010 V
transition	B 1011 4 0100	D 1101 6 0110	8 1000 1 0001
faults	X3 / 1	X3 / 1 , X2 / 1	X3 / 1, X2 / 1, X1 / 1

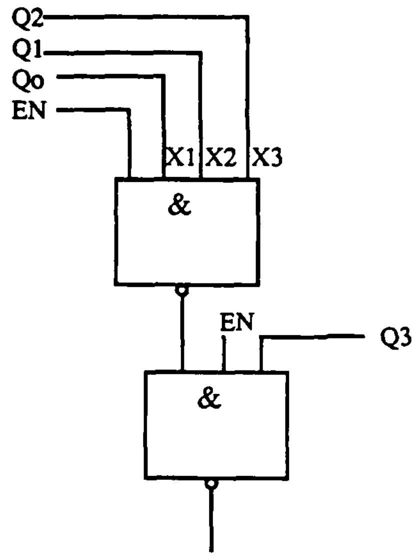


Fig. A.2: Faults for 74LS163, Vendor B, Low Voltage, Room Temperature.

APPENDIX A.3

Waveforms for the 74LS32

Figure A.3 shows the waveforms observed on the 74LS32. The experimental set-up is described in Fig. 11. Each figure shows the 74LS32 input (X Y) and output (V_{out}) waveforms. The numbers on the X waveform are a representation of the orders the input vectors are applied to the OR gate: 0 3 2 1 means (X Y) = (00) (11) (10) (01). Notice that the errors (glitches in the V_{out} waveforms) always occur when vector 2 or 3 is applied; whichever is applied first.

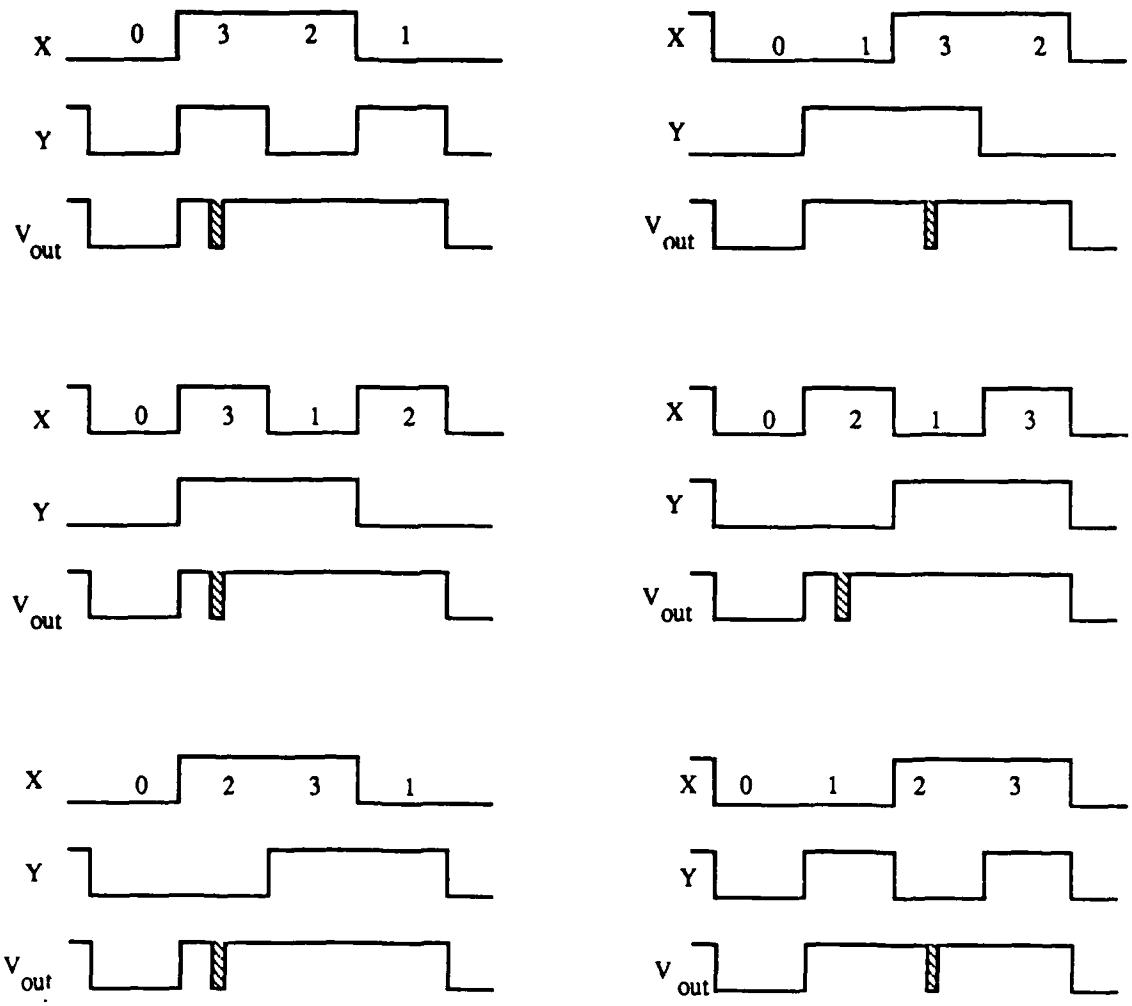
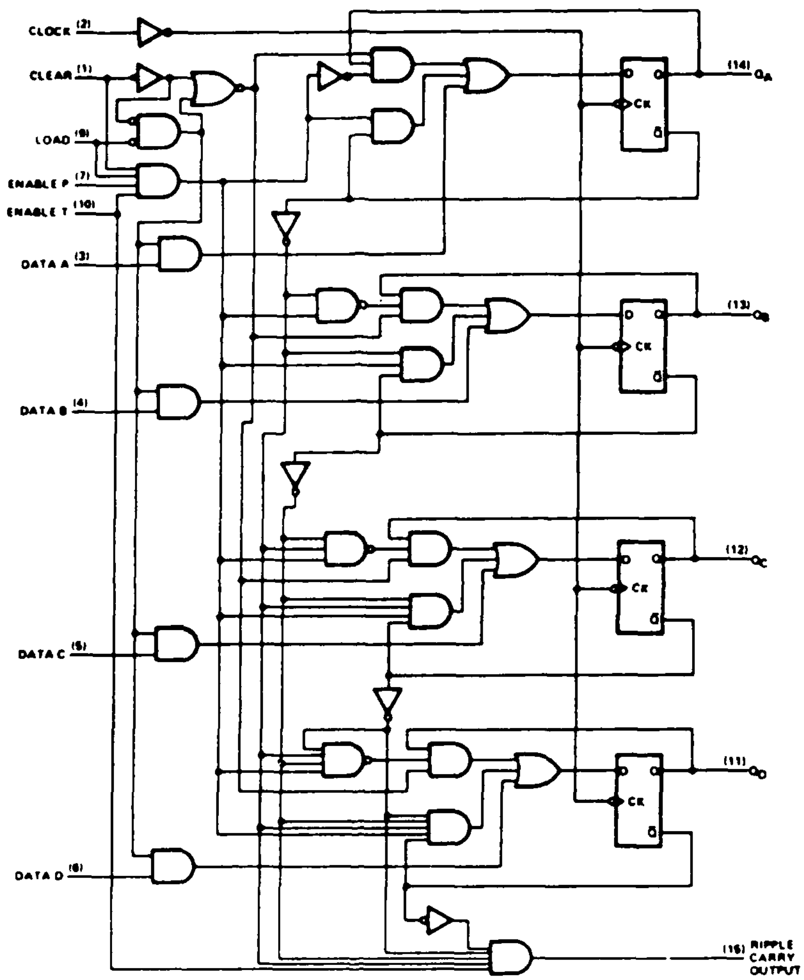


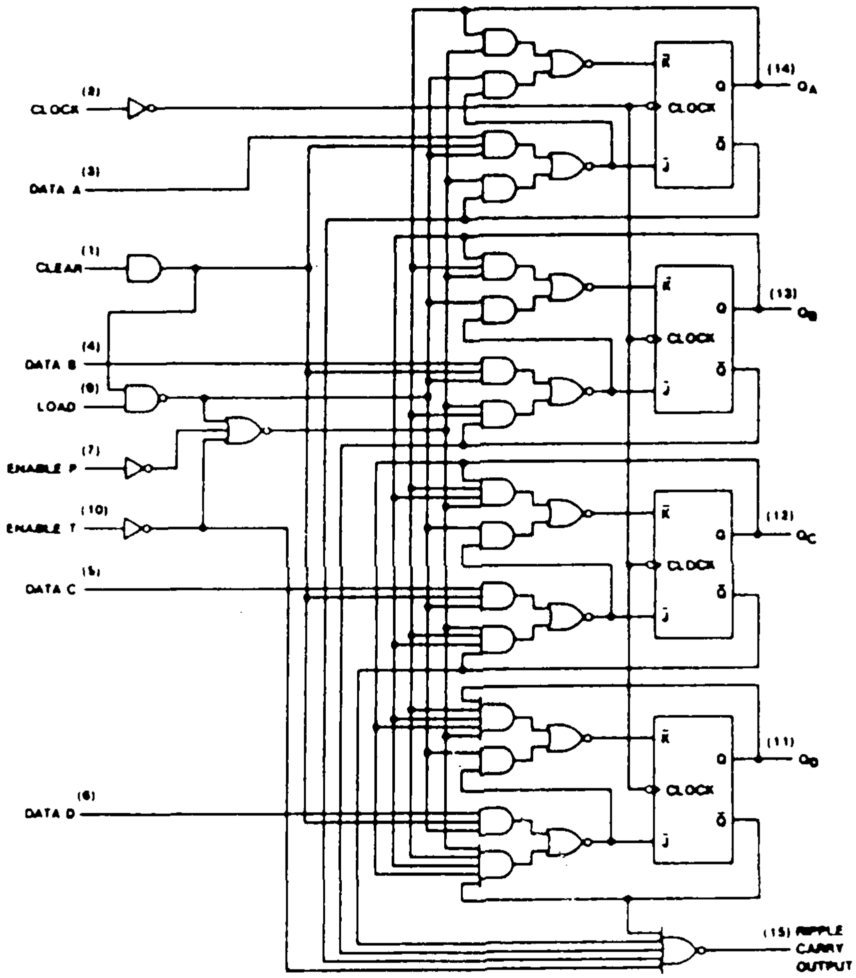
Fig. A.3: Waveforms for the 74LS32.

APPENDIX A.4

Logic Diagram of the Counters



Binary Counter 74LS163; Vendors B and C.



Binary Counter 74LS163; Vendor D.

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